

In re Application of:

Examiner: D. Kang

Art Unit: 2811

For: TRANSISTOR AND LOGIC CIRCUIT
ON THIN SILICON-ON-INSULATOR WAFERS
BASED ON GATE INDUCED DRAIN
LEAKAGE CURRENTS

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir or Madam:

Prior to examination of the above referenced application, Applicant respectfully request the Examiner to cancel Claims 1-10 and 19-26.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR and ZAFMAN

Dated:

5/24/01

Chun M. Ng
Reg. No. 36,878